REMARKS

Claims 16-19, 21-24 and 26-33 are pending in this application. Claims 1-15, 20, and 25 were previously cancelled, and claims 29-33 were previously withdrawn. Claims 16, 17, and 24 have been amended herein. In view of these amendments and remarks, Applicants respectfully request reconsideration of the claims.

The Office Action objected to the amendments to the specification filed on 12/22/2006, 4/24/2007, and 5/1/2009 under 35 U.S.C. § 132(a) as introducing new matter into the disclosure. Particularly, the Office Action objects to any reference of Figure 1j as introducing new matter. *See* Final Office Action p. 12 (mailed 12/3/2008). Further, the Office Action objected to the drawings, particularly, amended Figure 1j filed on 6/24/2008, as introducing new matter. The Office Action states, "For example, in figure 1j, spacer layers 132 having thinner regions along sides of the gate electrode and the gate dielectric is a new matter." Office Action p. 2.

Applicants respectfully reassert all previous arguments with regard to this issue and further add the following remarks.

Paragraphs [0024] and [0025], as originally filed, and portions of Figures 1d-e are reproduced below for convenience.

> **[0024]** FIG. 1e illustrates the wafer 100 of FIG. 1d after the first dielectric layer 126 (FIG. 1d) has been patterned to form notched spacers 132. The first dielectric layer 126 may be patterned, for example, by performing a timed isotropic wet etch process using a solution of dilute hydrofluoric acid. The height of the notch will depend on the thickness of the first dielectric layer, the etch rate of the first dielectric layer, and etch duration.
>
> **[0025]** As illustrated in FIG. 1e, the portion of the first dielectric layer 126 (FIG. 1d) located under the notched-spacer masks 130 is removed due to the isotropic etch process, thereby creating a notched spacer. The width of the notch will be dependent upon the thickness of the first dielectric layer 126 and the notch height may be controlled by varying the etch duration. Furthermore, FIG. 1e illustrates the situation in which the first dielectric layer 126 is removed completely to the gate electrode 122. In other situations, a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122. This may be desirable, for example, when it is preferred to control the depth and angle of

the implant or to protect the gate electrode 122 or gate dielectric 120 from damage during the etching process or other processes.

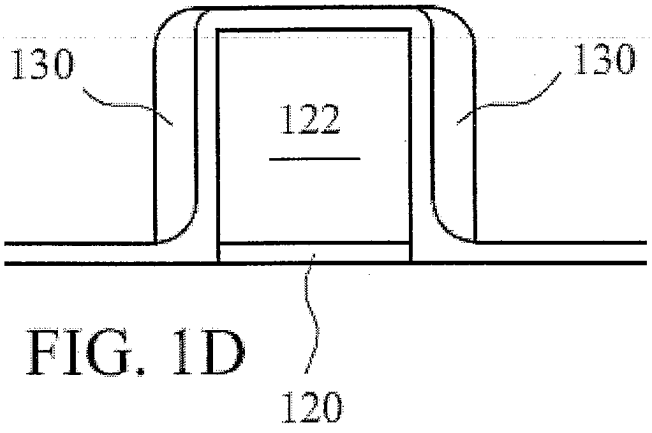


FIG. 1D

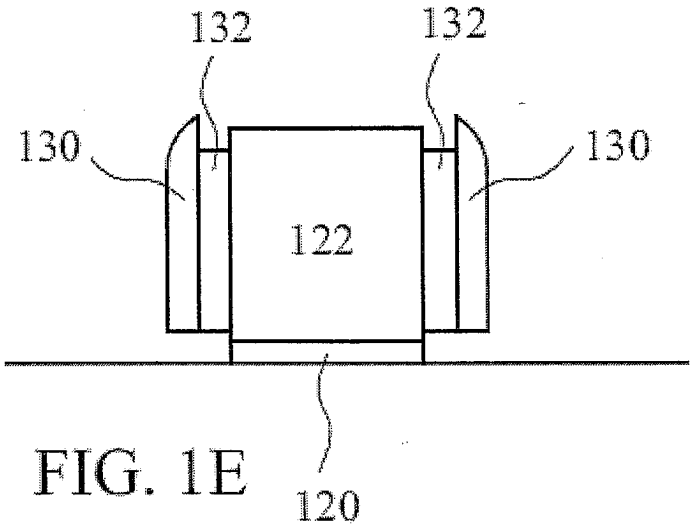


FIG. 1E

As discussed in the above recited paragraphs, the first dielectric layer 126 is etched with a wet etching, which causes the portion of the first dielectric layer 126 located under the notched-spacer masks 130 to be removed. As is known by a person having ordinary skill in the art, the isotropic etch for the first dielectric layer 126 on the substrate surface and covered by the mask

130 would proceed substantially laterally, or in other words, parallel to the substrate surface, from the exposed side of the mask 130 towards the gate electrode 122.

Later sentences in paragraph [0025] reveal examples of the results of this isotropic etch. For example, Figure 1e illustrates an embodiment where the entire portion of the first dielectric layer 126 on the surface of the substrate and under the mask is removed. Applicants' specification then states that "[i]n other situations, a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122." This example illustrates that the Applicants had possession of the example depicted in Figure 1j, where "a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122." Thus, in context, this illustrates that Applicants had possession of laterally etching the first dielectric layer 126 under the mask 130 and on the substrate surface such that a portion of the first dielectric layer 126 remains on the side of the gate electrode 122. This is what is depicted in Figure 1j, and as shown, is clearly described by the specification as filed. Accordingly, Figure 1j and any references to Figure 1j do not add new matter.

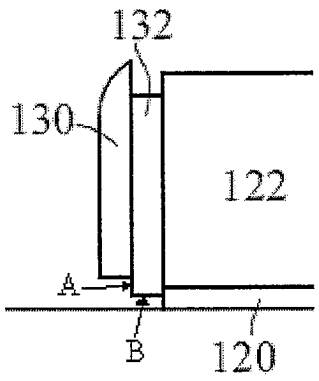
The Office Action states that Applicants arguments with respect to the 112 rejections based on a lack of written description, which would be obviated by a finding that Figure 1j does not add new matter, were addressed in a previous office action. Office Action p. 18. Applicants assume that the Office Action is referring to the Final Office Action mailed on 12/3/2008. Applicants address the Examiner's Response to Arguments herein.

The Final Office Action asserted:

> The recitation of "a portion of the notched spacer is completely, or partially removed along the corner formed between the surface of the substrate and the gate electrode sidewall" does not necessarily mean that the notched spacer is thinner along the surface of the substrate. Partially removing a portion of the notched spacer along the corner formed between the surface of the substrate and the gate electrode sidewall, can mean that an entire small portion

> of spacer is removed along the corner, thus leaving another portion of the spacer, which is not covered by the mask, intact. There is certainly no support for the top of the thinner spacer being aligned with the bottom of the mask, as depicted in figure 1j.

Final Office Action p. 13-14. Applicants interpret the example posited by the Final Office Action, what the recitation "could mean," as depicted below.



Hypothetical of Final Office Action as Interpreted by Applicants

Applicants do not understand this example given by the Final Office Action, assuming Applicants' interpretation is correct. In context of the specification, particularly paragraphs [0024]-[0025], Applicants do not understand how the isotropic etch process would result in the depicted structure. Particularly, how could the portion of the first dielectric layer 126 underlying surface B be etched but surface A of the first dielectric layer 126 would remain unaffected when the material at surface A is the same material underlying surface B before the etch? Applicants respectfully submit that given the processes and procedures disclosed in the specification, one of ordinary skill in the art would not understand that the hypothetical structure suggested by the Office Action would be achieved, but rather, would understand that the structure illustrated in Figure 1j would be achieved.

Further, the above hypothetical would not accomplish the desired functions of when "a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122" to

further evidence that the hypothetical is not a correct interpretation of the specification. The specification states in reference to when "a portion of the first dielectric layer 126 may remain" that "[t]his may be desirable, for example, when it is preferred . . . to protect the gate electrode 122 or gate dielectric 120 from damage during the etching process or other processes." In the above hypothetical, the gate dielectric 120, and in some situations a portion of the gate electrode, is exposed, and thus, would not be protected during etching or other processes. However, the example depicted in Figure 1j would obtain this desired effect because neither the gate electrode 122 nor the gate dielectric 120 is exposed, and thus, they are both protected. Accordingly, the Examiner's hypothetical is an incorrect interpretation of the specification, and a person having ordinary skill in the art would understand the recited passage to describe the embodiment depicted in Figure 1j.

The Final Office Action also asserted:

> Note that the phrase "a notched spacer is thinner along the surface of the substrate" is not synonymous to the phrase "a notched spacer is thinner at a first portion closer to the surface of the substrate than at a second portion being further from the substrate".

Final Office Action p. 13. Applicants respectfully disagree. The recitation "the notched spacer is thinner along the surface of the substrate" is stated with reference to "forming a notched spacer." An embodiment of the "forming of a notched spacer" is described in the specification in paragraphs [0024]-[0025], as discussed above. In the context of this formation, an isotropic etch is used to form the notched spacer. The portion that is removed, as described in those paragraphs and in Figure 1d-e, or partially removed, as also described in the text, is clearly "a first portion closer to the surface of the substrate than a second portion being further from the substrate." Accordingly, the assertion of the Final Office Action has no merit.

Therefore, because when the descriptions in paragraphs [0024]-[0025] and the features in original claim 16 are properly placed into context, Figure 1j is fully supported by the original specification, and Figure 1j does not add any new matter. Accordingly, Applicants respectfully request that the objections be withdrawn.

The Office Action objected to claims 24 and 26-28 because of informalities. Particularly, the Office Action asserted, "The phrase 'the surface of the substrate', as recited in claim 24, should read 'a surface of the substrate.'" Without conceding the merits of the objection and to expedite prosecution of the application, Applicants have amended claim 24 as suggested by the Office Action. Accordingly, Applicants respectfully request that the objection be withdrawn.

The Office Action rejected claims 16-19, 21-24 and 26-28 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Applicants respectfully traverse this rejection.

Claims 16 and 24 are fully supported by Figure 1j, which, as discussed above, was fully supported by the originally filed specification, and corresponding paragraphs [0024]-[0025]. Accordingly, Applicants respectfully submit that claims 16-19, 21-24, and 26-28 are described or illustrated by paragraphs [0024]-[0025] and Figure 1j such that a person having ordinary skill in the art would understand that Applicants had possession of the inventions of claims 16-19, 21-24, and 26-28 at the time the application was filed. Therefore, Applicants respectfully request that the rejection be withdrawn.

The Office Action rejected claims 17-19, 24 and 26-28 under 35 U.S.C. § 112, second paragraph, as assertedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office Action stated that different features in claims 17 and 24 were "unclear." *See* Office Action p. 5. Without

conceding the merits of the rejection and to expedite prosecution of the application, Applicants have amended claims 17 and 24 to clarify the scope of the respective claims. Applicants respectfully submit that the amendments have clarified any feature that the Office Action asserts as "unclear," and accordingly, Applicants respectfully request that the rejection be withdrawn.

The Office Action rejected claims 16 and 21-23 under 35 U.S.C. § 103(a) as assertedly being unpatentable over Schuegraf et al. (U.S. Patent No. 7,009,264, hereinafter "Schuegraf") in view of Boissonnet et al. (U.S. Patent No. 7,015,105, hereinafter "Boissonnet") or Nishinohara et al. (U.S. Patent No. 6,911,705, hereinafter "Nishinohara"). The Office Action rejected claims 17-19 under 35 U.S.C. § 103(a) as assertedly being unpatentable over Schuegraf, Boissonnet and Nishinohara, as applied to claim 16, and further in view of Chen et al. (U.S. Patent No. 6,610,571, hereinafter "Chen"). Applicants respectfully traverse these rejections.

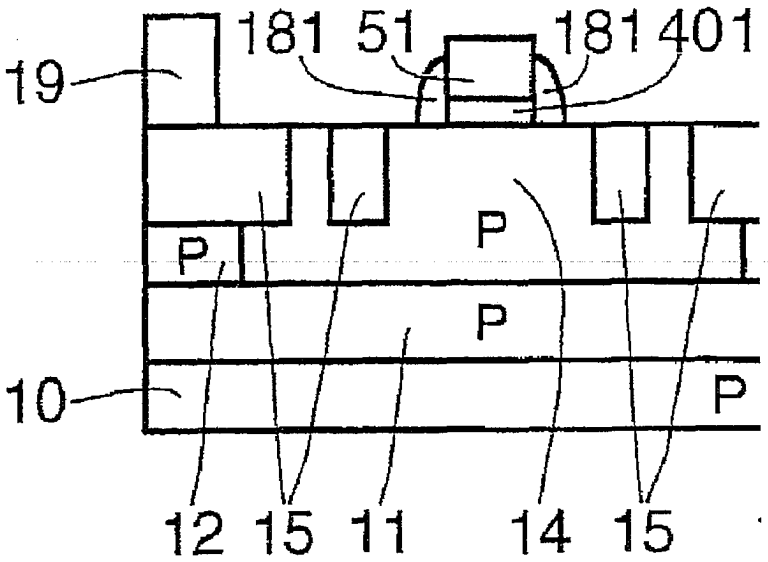
Applicants respectfully submit that the asserted combinations of Schuegraf and Boissonnet or Nishinohara fail to teach or suggest all of the features of claim 16, and that claim 16 is allowable over these cited references. Claim 16 recites "performing a first ion implant at an oblique angle to the substrate so as to implant ions beneath the gate electrode wherein the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type," which first conductivity type is the same conductivity type of the region in the substrate on which the gate electrode is formed. The asserted combinations fail to teach or suggest these features.

The Office Action admits that "Schuegraf et al. do not teach performing a first ion implant at an oblique angle to the substrate so as to implant ions beneath the gate electrode wherein the gate electrode and the notched spacer acts as masks during the first ion implant, the first ion implant using ions of the first conductivity type." Office Action p. 6.

However, the Office Action asserted that Boissonnet taught these features. Particularly, the Office Action asserted that "Boissonnet et al. teach in figures 12 and 13 and related text performing a first ion implant 22 at an oblique angle to the substrate so as to implant ions beneath the gate electrode 51 wherein the gate electrode 51 and the notched spacer 181 act as masks during the first ion implant, the first ion implant using ions of the first conductivity type." Office Action p. 6-7. Applicants respectfully traverse this assertion.

Boissonnet teaches forming P-type wells 13 and 14 in a substrate 1. Boissonnet col. 2, lines 53-62; Figure 1 (P-type well 13 is labeled 12 in the figure). Boissonnet then teaches, with reference to Figure 12, that a second dopant 22 is implanted, that the implantation is oblique, and that the second dopant is arsenic or phosphorus. Boissonnet col. 4, lines 1-17. Arsenic and phosphorus are both well-known n-type ion dopants. Thus, the asserted "first ion implant 22" is of a different conductivity type than the region in the substrate 1 on which the gate 51 is formed. Accordingly, the asserted "first ion implant 22" does not "us[e] ions of the first conductivity type" wherein "the first conductivity type" refers to the conductivity type of the region in the substrate on which the gate electrode is formed.

Further, Boissonnet teaches the formation of spacers 181. Boissonnet col. 3, lines 53-60. These spacers 181 are illustrated in Figure 12, of which a portion is reproduced below for convenience.



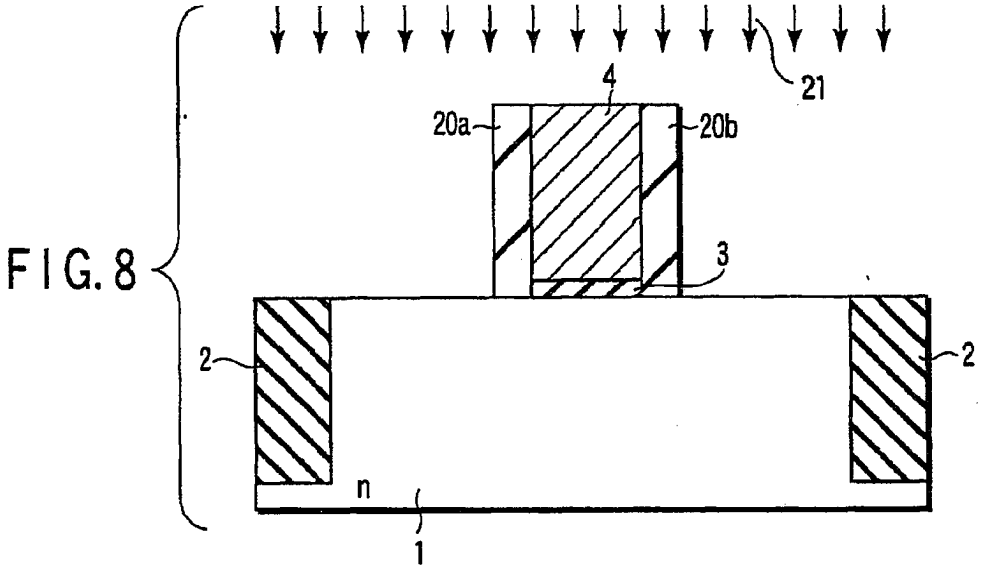
Boissonnet Figure 11 (portion)

As recited above, the Office Action asserted that "the notched spacer 181 act as masks during the first ion implant [22]." Applicants' claim 16 recites that "the notched spacer" has "a first thickness in an upper portion and a second thickness less than the first thickness in a lower portion adjacent to a surface of the substrate thereby forming a notch in the lower portion of the notched spacer." As can be seen from the reproduced portion of Figure 11, Boissonnet does not teach a "notched spacer" because spacer 181 has a first thickness in an upper portion that not only does not have a second thickness less than the first thickness in a lower portion adjacent to the surface of the substrate, but has a second *greater* thickness in the lower portion. Therefore, Boissonnet cannot teach a "notched spacer", and thus, does not teach that a "notched spacer act[s] as [a] mask[] during the first ion implant," as recited in Applicants' claim 16.

Therefore, neither Schuegraf nor Boissonnet, either individually or in combination, teaches or suggests all of the features of claim 16, and Applicants respectfully submit that claim 16 is allowable over the asserted combination of Schuegraf and Boissonnet.

The Office Action further asserted that "Nishinohara teach[es] in figures 8 and 9 and related text (column 8, lines 52-63) performing a first ion implant . . . wherein the gate electrode 4 and the notched spacer 20a act as masks during the first ion implant." Office Action p. 7. Applicants respectfully traverse this assertion.

Nishinohara teaches the formation of offset spacers 20a and 20b. Figure 8 of Nishinohara illustrates these spacers and is reproduced below for convenience.



Nishinohara Figure 8

As seen from Figure 8, offset spacers 20a and 20b have a uniform thickness alongside gate electrode 4. Thus, the offset spacers 20a and 20b cannot be a "notched spacer" because offset spacers 20a and 20b have a uniform thickness in an upper portion and in a lower portion adjacent to the surface of the substrate, and not "a first thickness in an upper portion and a second thickness less than the first thickness in a lower portion adjacent to a surface of the substrate." Therefore, Nishinohara cannot teach a "notched spacer," and thus, does not teach that a "notched spacer act[s] as [a] mask[] during the first ion implant," as recited in Applicants' claim 16. Therefore, neither Schuegraf nor Nishinohara, either individually or in combination, teaches or

suggests all of the features of claim 16, and Applicants respectfully submit that claim 16 is allowable over the asserted combination of Schuegraf and Nishinohara.

The Office Action rejected claims 16 and 21-23 under 35 U.S.C. § 103(a) as assertedly being unpatentable over Singh et al. (U.S. Patent No.6,417,084, hereinafter "Singh") in view of Boissonnet or Nishinohara. The Office Action rejected claims 17-19 under 35 U.S.C. § 103(a) as assertedly being unpatentable over Singh, Boissonnet and Nishinohara, as applied to claim 16, and further in view of Chen. Applicants respectfully traverse these rejections.

Applicants respectfully submit that the asserted combinations of Singh and Boissonnet or Nishinohara fail to teach or suggest all of the features of claim 16, and that claim 16 is allowable over these cited references. The Office Action admitted that Singh does not teach "performing a first ion implant . . . wherein the gate electrode and the notched spacer act as a mask during the first ion implant," but asserted that both Boissonnet and Nishinohara teach performing a first ion implant with the elements and associated features exactly as recited above with the previous rejection. Office Action p. 10. For the same reasons as discussed above, Boissonnet fails to teach or suggest that "the first ion implant us[es] ions of the first conductivity type" and that a "notched spacer act[s] as [a] mask[] during the first ion implant." Further, for the same reasons as discussed above, Nishinohara fails to teach or suggest that a "notched spacer act[s] as [a] mask[] during the first ion implant." Accordingly, neither Singh nor Boissonnet, either individually or in combination, teach or suggest all of the features of claim 16, and neither Singh nor Nishinohara, either individually or in combination, teach or suggest all of the features of claim 16. Therefore, Applicants respectfully submit that claim 16 is allowable over the cited references.

Claims 17-19 and 21-23 depend from claim 16 and add further defining features. Applicants respectfully submit that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding further features.

The Office Action rejected claims 24 and 26-28 under 35 U.S.C. § 103(a) as assertedly being unpatentable over Schuegraf in view of Boissonnet, Nishinohara and Chen. Applicants respectfully traverse this rejection.

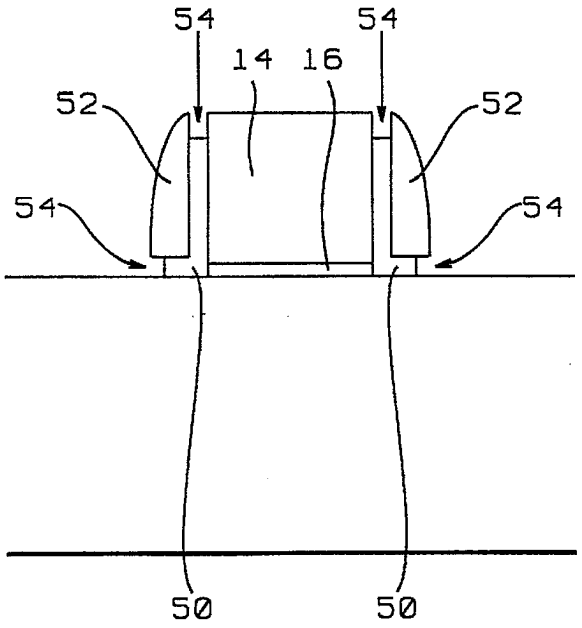
Applicants respectfully submit that Schuegraf specifically teaches away from the asserted combination and from the claimed features. Claim 24 recites:

> forming a first layer having a first thickness over the substrate and the gate electrode;
>
> . . .
>
> isotropically etching the first layer to form a notched spacer in the first layer.

Despite the Office Action's assertion that Schuegraf teaches these features, Office Action p. 14, Schuegraf expressly teaches away from these features. Schuegraf teaches, "In the second step, represented in FIGS. 2B and 2C, a *selective* spacer 210 is deposited . . . leaving the active area 215 free of deposition," and further, "Because the spacer is *selectively deposited* there is *no need for an additional etch step to remove excess spacer material.*" Schuegraf col. 3, lines 23-27, 33-35 (emphasis added). Not only does Schuegraf not teach the formation of a first layer over a substrate, Schuegraf explicitly teaches that no first layer is formed over the substrate because the spacer 210 is formed by a selective deposition. Further, Schuegraf teaches away from ever etching spacer 210 because doing so is unnecessary because of the selective deposition. Accordingly, Schuegraf teaches away from the claimed features, and any obviousness rejection of claim 24 based on any combination of references including Schuegraf is improper.

Further, Applicants respectfully submit that the remaining references fail to teach or suggest all of the features of claim 24 such that claim 24 is allowable over the remaining references. Claim 24, as amended, recites "isotropically etching the first layer to form a notched spacer in the first layer, . . .wherein the etching partially removes the lower portion of the first layer thereby forming a notch in the notched spacer such that the notched spacer has a second thickness in a direction substantially orthogonal to the sidewall of the gate electrode along the surface of the substrate that is less than the first thickness." The Office Action asserted that Chen taught "etching the first layer to form a notched spacer . . . ." Office Action p. 15. Applicants respectfully traverse this assertion.

Chen fails to teach forming a "notched spacer" having "a second thickness in a direction substantially orthogonal to the sidewall of the gate electrode along the surface of the substrate that is less than the first thickness." Figure 4 of Chen is reproduced below for convenience.



Chen Figure 4

Assumedly, the Office Action asserts layer 50 as the "notched spacer." However, as can be clearly seen from Figure 4, the thickness of layer 50 along the substrate 10 in a direction substantially orthogonal to the sidewall of the body 14 of the gate electrode is greater than the thickness of layer 50 as originally formed. Accordingly, Chen fails to teach or suggest the asserted features.

Likewise, for similar reasons as discussed above with regard to claim 16, both Boissonnet and Nishinohara fail to teach or suggest a "notched spacer." Accordingly, any asserted combinations of Chen, Boissonnet, and Nishinohara fail to teach or suggest all of the features of claim 23, and Applicants respectfully submit that claim 23 is allowable over the cited references.

As an auxiliary matter, and to clarify and narrow the issues in proceeding with the prosecution of the current application, Applicants respectfully submit that Boissonnet does not teach or suggest the features asserted by the Office Action. The Office Action asserted that Boissonnet teaches "performing a first ion implant 22 . . .the first ion implant using ions of the first conductivity type." Office Action p. 14-15. For similar reasons as discussed above with regard to claim 16, Boissonnet does not teach these features, but teaches an implant using N-type impurities when the substrate is of a P-type conductivity, i.e. the "first conductivity type." Accordingly, Boissonnet does not teach the features asserted by the Office Action.

Claims 26-28 depend from claim 23 and add further defining features. Applicants respectfully submit that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding further features.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Steven H. Slater, Applicants' attorney, at 972-732-1001, so that such issues may be resolved as expeditiously as possible. The Commissioner is hereby authorized to charge any fees that are due, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

12 OCT 2005
Date

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